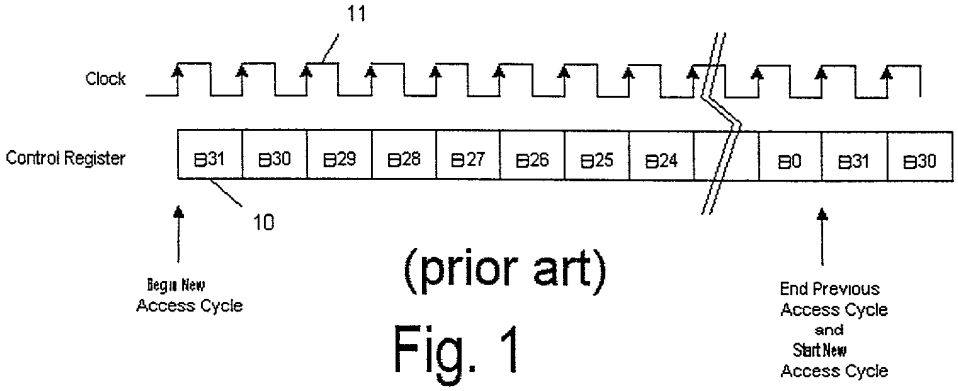


(prior art)

Fig. 1

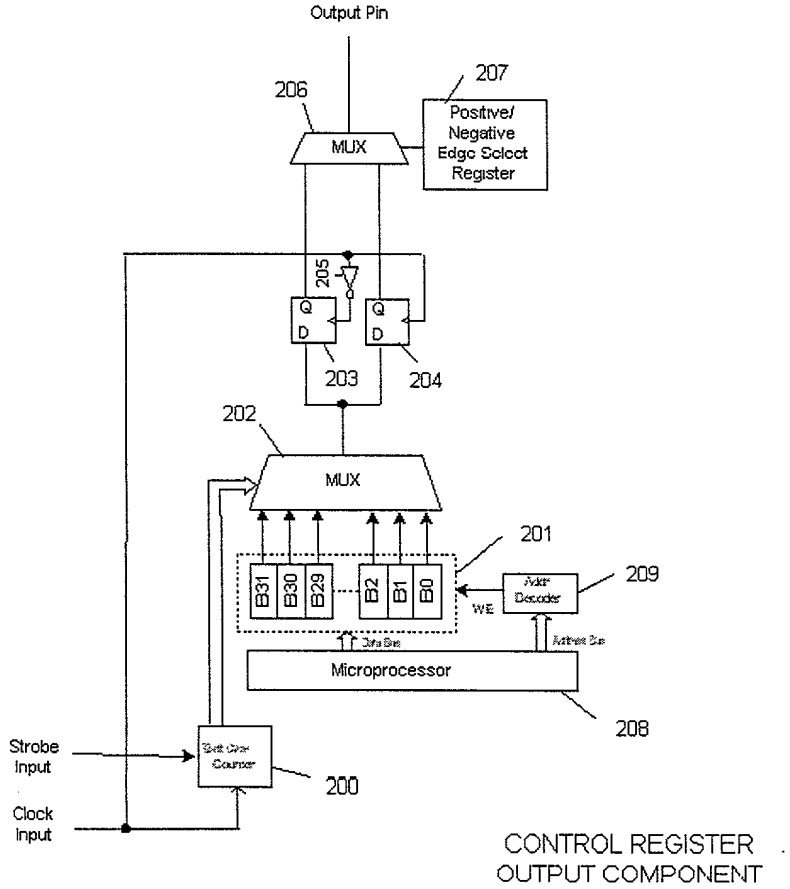


Fig. 2

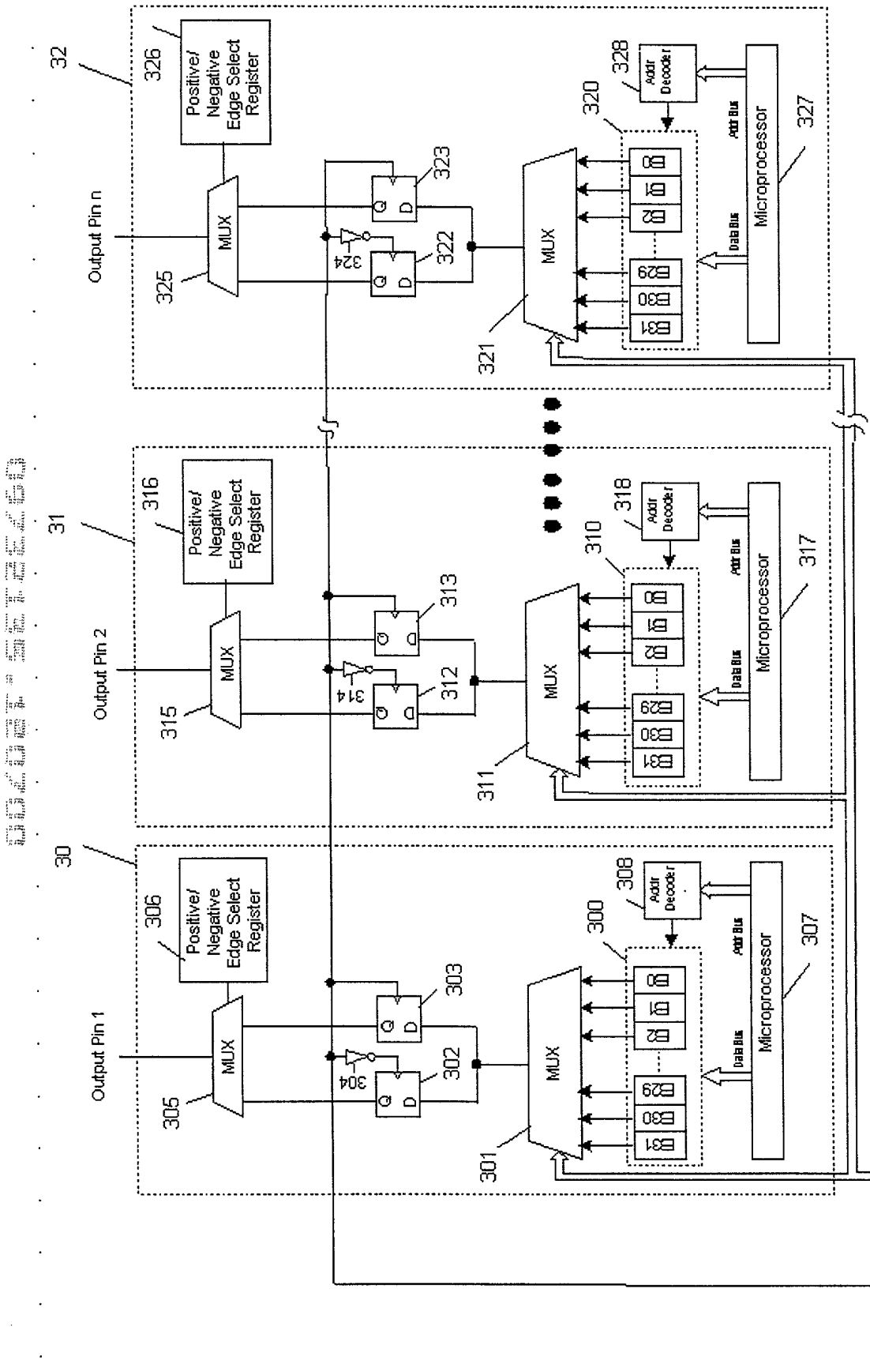


Fig. 3

CONTROL REGISTER
OUTPUT COMPONENTS
CONNECTED ON A BUS

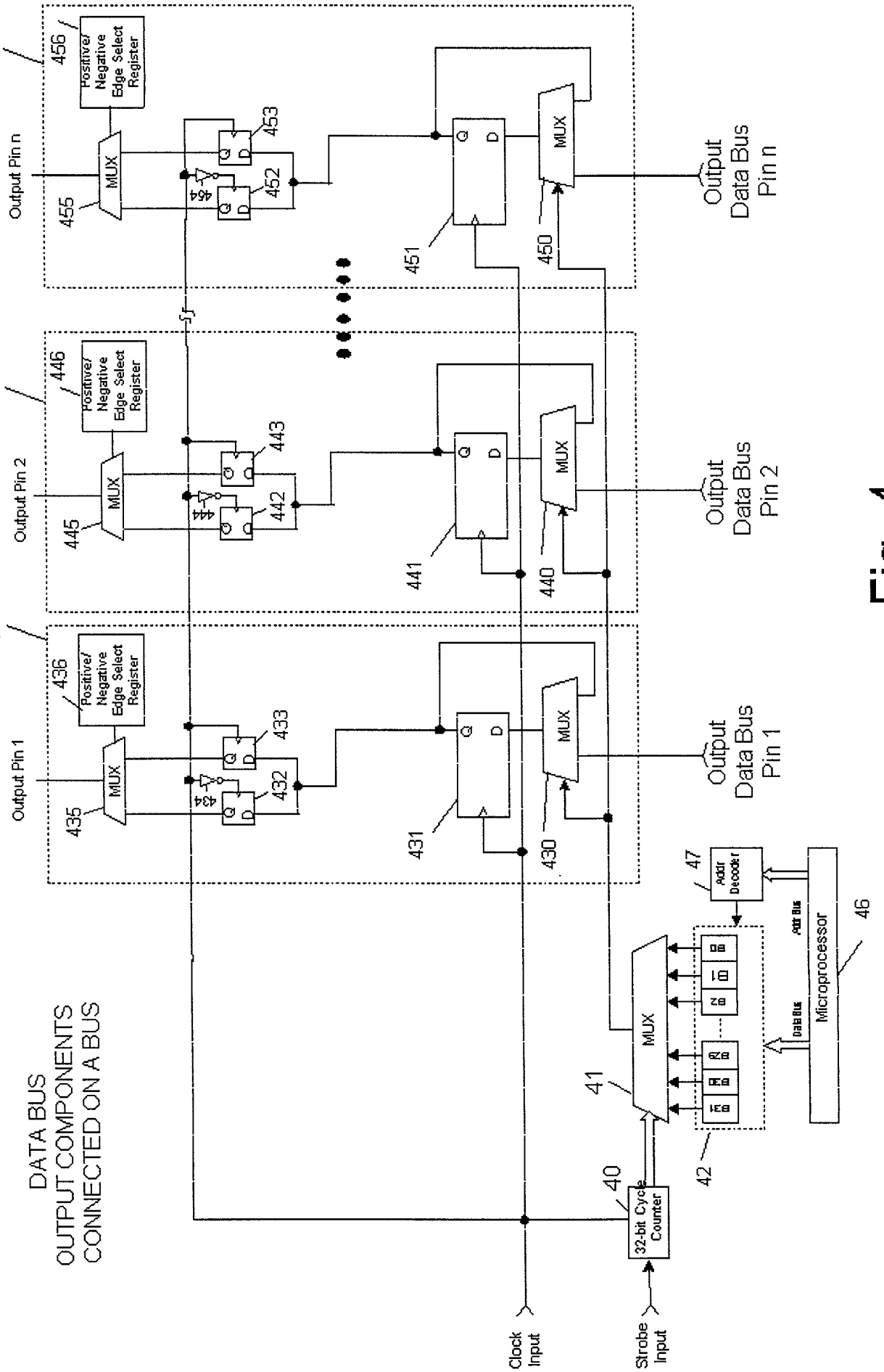
DATA BUS
OUTPUT COMPONENTS
CONNECTED ON A BUS
Output Pin n
Output Pin 2
Output Pin 1
Positive/ Negative Edge Select Register
MUX
Output Data Bus Pin n
Output Data Bus Pin 2
Output Data Bus Pin 1
32-bit Cycle Counter
Clock Input
Strobe Input
Addr Decoder
Addr Bus
Data Bus
Microprocessor

Fig. 4

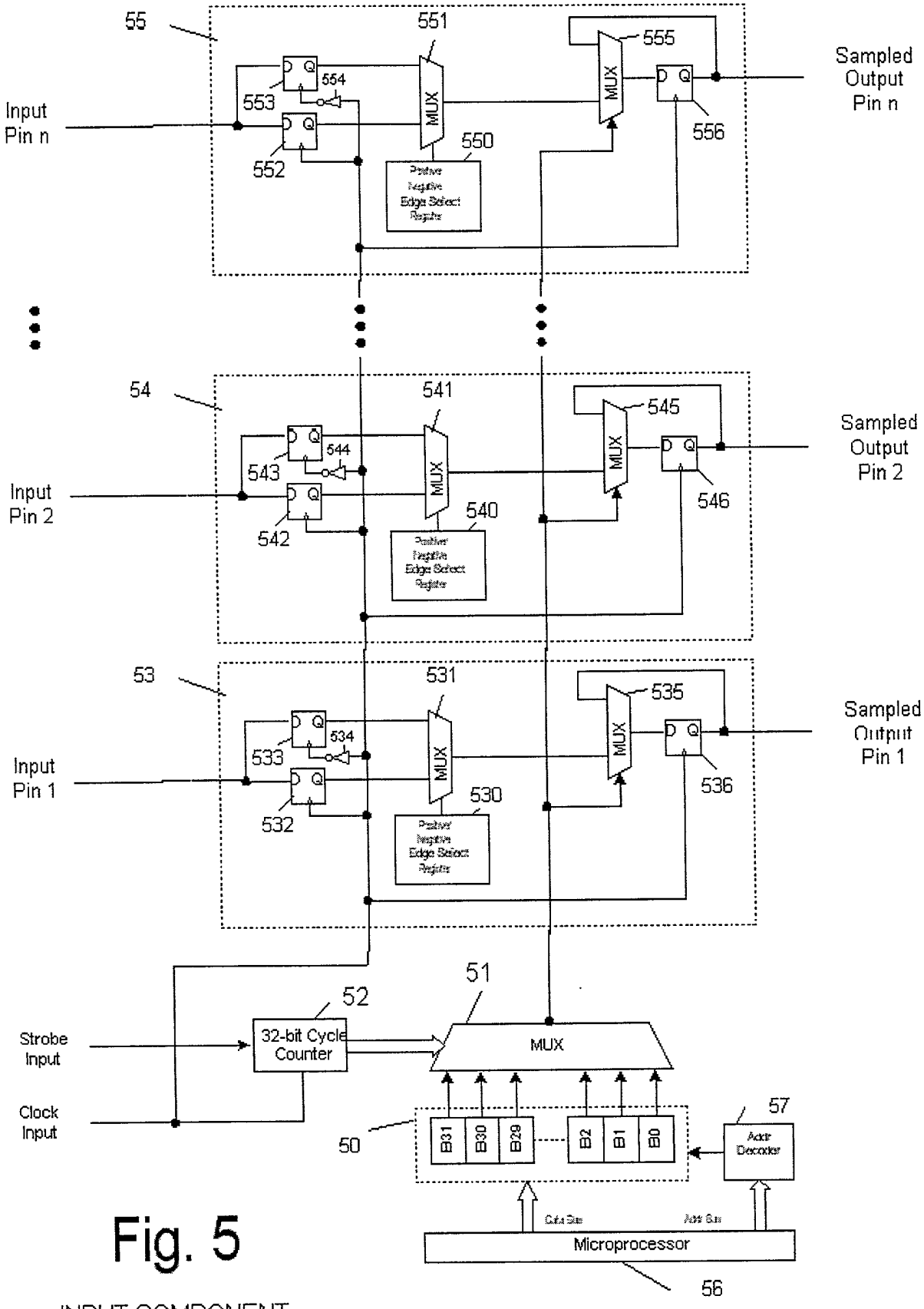


Fig. 5

INPUT COMPONENT

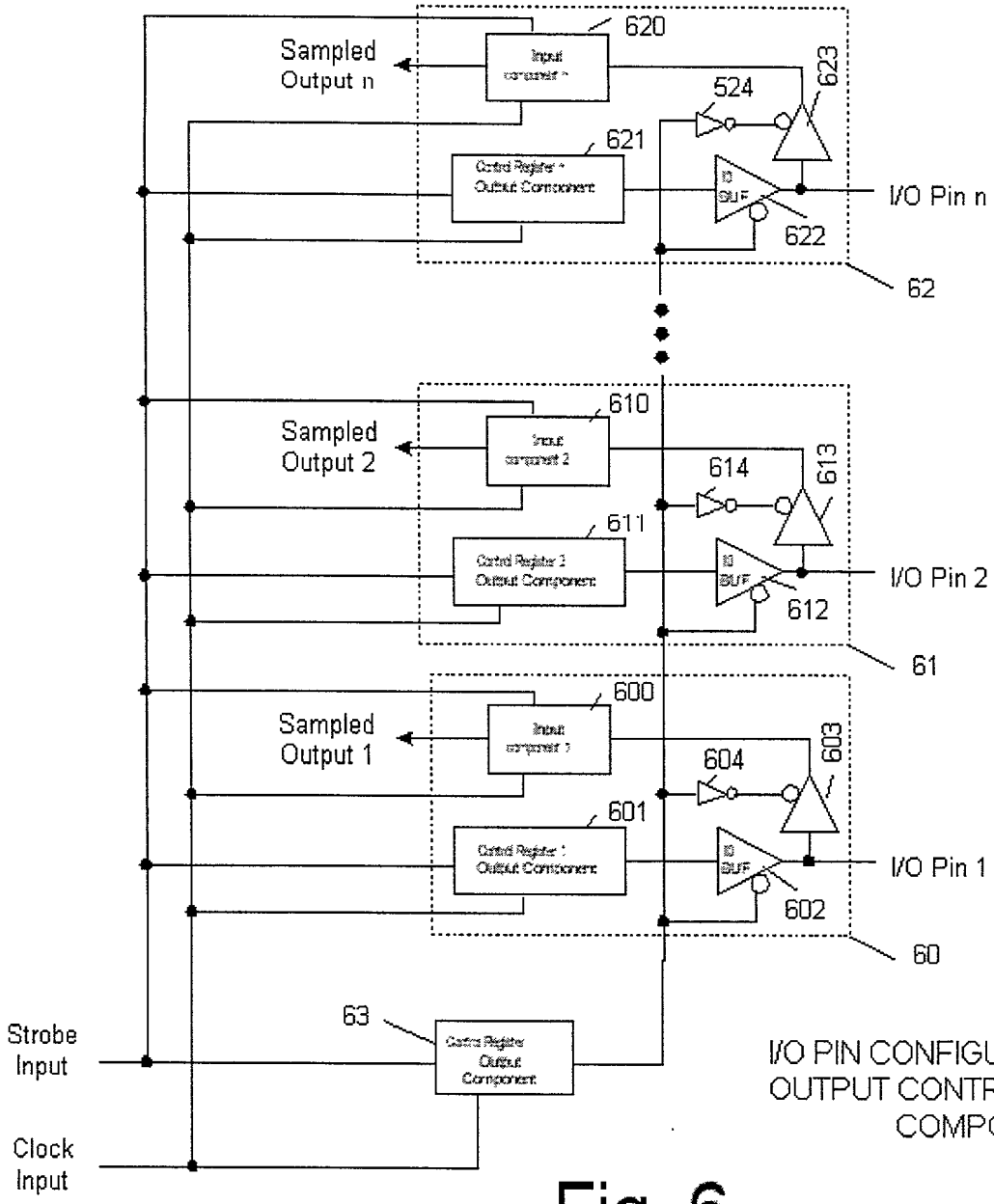
Sampled Output n
620
623
524
621
I/O Pin n
622
62
Sampled Output 2
610
613
614
611
I/O Pin 2
612
61
Sampled Output 1
600
603
604
601
I/O Pin 1
602
60
Strobe Input
63
Clock Input
I/O PIN CONFIGURATION
OUTPUT CONTROL REG
COMPONENT

Fig. 6

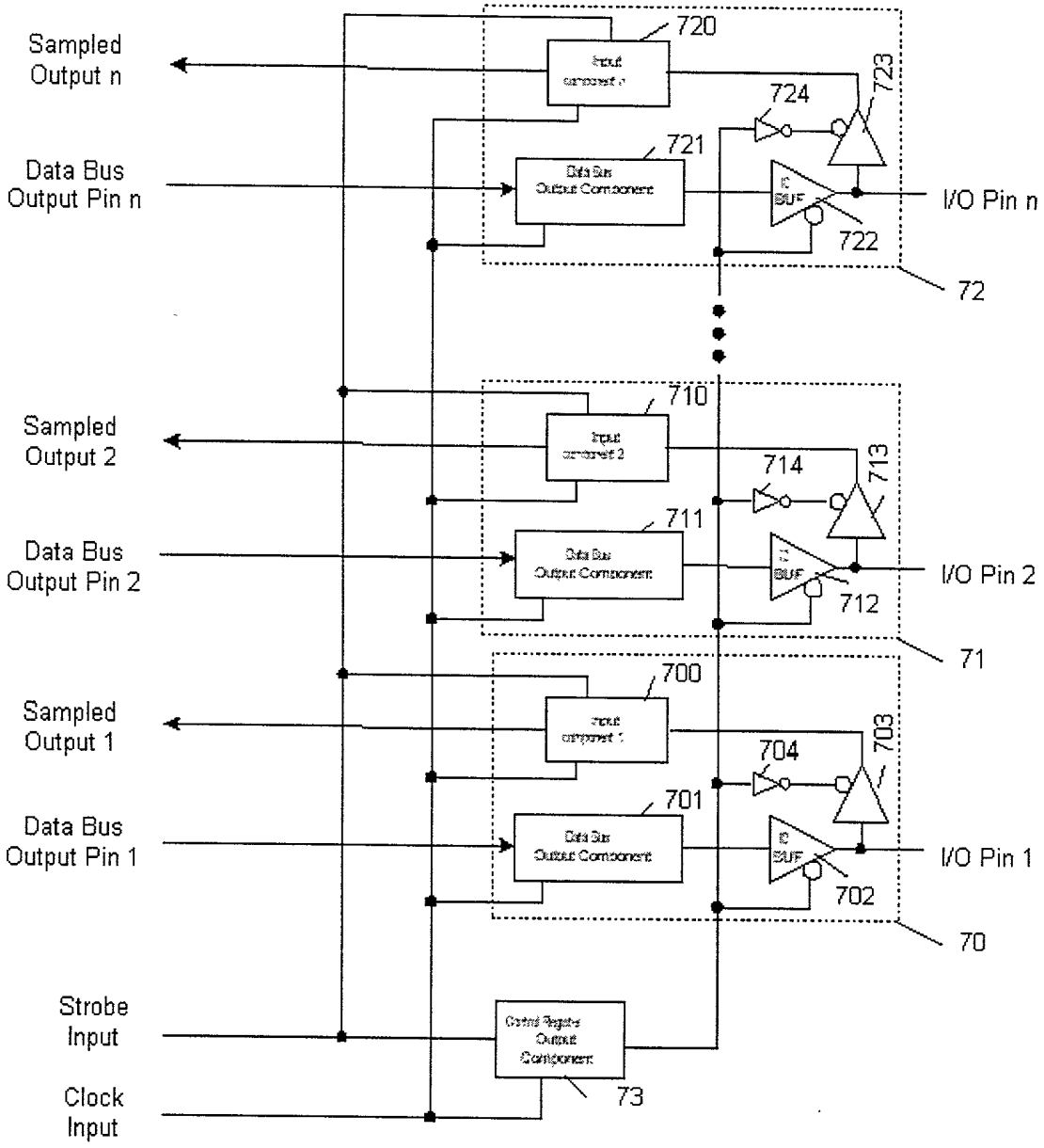


Fig. 7

I/O PIN CONFIGURATION
FOR OUTPUT DATA BUS